

Call For Papers
**IEEE/ACM International Symposium on Nanoscale Architectures
(NANOARCH'07)**

Co-located with IEEE International Test Conference

October 21-22, 2007

Santa Clara, CA, USA

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Moore's law based scaling is rapidly approaching a "brick wall" as we enter the nanoelectronic regime. Novel silicon and non-silicon nanoelectronic devices are being developed to explicitly address this problem. Similarly, while defect and fault-tolerance techniques are designed under the assumption that a system is composed largely of correctly functioning units, this is no longer true in emerging nanoelectronics. In addition, nanoelectronics offers massive parallelism on a scale significantly beyond anything we have seen before, yet very few commercial massively parallel applications are envisioned. Also, while current computer aided design tools and methodologies can barely manage billion-transistor chips, how can trillion-device chips that nanoelectronics promises be designed? The purpose of the NANOARCH symposium is to be a forum for the presentation and discussion of novel architectures and design methodologies to address these issues of nanoscale implementation. NANOARCH is interested in novel architectures including massively parallel, biologically inspired as well as those that are defect and fault tolerant, case studies on defect, fault and yield models, experimental reliability evaluation, validation frameworks, computer aided simulation, and design tools and emerging computational models for nanoelectronics. Additional topics of interest include:

- Holistic architectures for nanoelectronic digital and mixed-signal circuits and systems
- Computational paradigms and programming models for nanoscale architectures
- Modeling and simulation of nanoelectronic devices, circuits and system architectures
- Simulation of complex systems with nanoscale computing architectures
- Implementing microarchitecture concepts using nanoarchitecture building blocks
- Defect and fault tolerant nanoelectronic device, circuit, and system level architectures
- Manufacture testing of nanoelectronic architectures
- Computer aided design tools and methodologies for nanoelectronic architectures

The Program Committee invites authors to submit papers up to 8 pages in length, describing original, unpublished recent work. Clearly describe the nature of the work, explain its significance, highlight novel features, and describe its current status. Electronic submission through the workshop website is required.

The submission of a paper proposal will be considered evidence that upon acceptance, the author(s) will present their paper at the workshop.

Final versions of accepted papers will be included in official IEEE/ACM NANOARCH symposium proceedings

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Important deadlines:

Submission deadline: August 6, 2007

Acceptance notification: Sept 7, 2007 Final version of papers: Sept 17, 2007

For up-to-date workshop information: <http://www.nanoarch.org>